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14EVE12

First Semester M.Tech. Degree Examination, Dec.2014/Jan.2015
Digital VLSI Design

Time: 3 hrs. Max. Marks:100

Note: *Answer any FIVE full questions.*

1 a. Derive the equations for Ids for all 3-regions starting from fundamentals. **(10 Marks)**

b. How do you change the above equation to reflect the effect of channel length modulation? **(04 Marks)**

c. Calculate Ids for nMOS enhancement transistor for following conditions:
i) $V_{us} = 0.7V$ ii) $V_{gs} = 2V$ $\lambda = 0$ iii) $V_{gs} = 2V$, $\lambda = 0.15/V$. Given:
$\mu_n = 600\ cm^2/V$, $C_{ox} = 7 \times 10^{-8}\ F/cm^2$, $V_{T_o} = 1V$, $V_{DS} = 5V$, W = 20μm, L = 20μm. **(06 Marks)**

2 a. Derive expressions for V_{IH}, V_{IL} and V_{th} for CMOS inverter. **(10 Marks)**

b. Derive the relation between $(W/L)_p$ and $(W/L)_n$ for symmetric CMOS inverter. Also discuss the effect of K_R variations on VTC. **(06 Marks)**

c. Discuss the enhancement load nMOS inverter. **(04 Marks)**

3 a. Define propagation delays and derive the expression for τ_{PHL} and τ_{PLH} for CMOS inverter using differential equation method. **(10 Marks)**

b. Explain 3-stage CMOS ring oscillator. **(06 Marks)**

c. Calculate the total resistance and total capacitance for uniform polysilicon line with length of 1000μm and a width of 4μm. Given: sheet resistance 30Ω/square, unit area capacitance $0.066fF/\mu m^2$, unit length capacitance 0.046 fF/μm. **(04 Marks)**

4 a. What is dynamic CMOS logic? Explain with aid of an example. **(06 Marks)**

b. Illustrate the cascading problem in a dynamic CMOS logic. How is it overcome? **(06 Marks)**

c. Discuss the dynamic voltage bootstrapping circuit with necessary mathematical equations. **(08 Marks)**

5 a. Discuss the 3-transistor DRAM cell with read and write operations. **(10 Marks)**

b. Explain memory structure SRAM with read and write circuitry with aid of read and write timing diagram. **(10 Marks)**

6 a. What is short circuit power dissipation? On what parameters does it depend? **(10 Marks)**

b. Describe the types of threshold CMOS circuits used to minimize dynamic power consumption in CMOS digital ICs. **(10 Marks)**

7 a. Differentiate between CMOS and BiCMOS. **(05 Marks)**

b. Explain the static characteristics of resistive load BJT inverter. **(07 Marks)**

c. Draw the BiCMOS circuits for the following with nMOS transistor for removing the base charge of bipolar transistor. i) $y = \overline{A}$ ii) $y = \overline{A + B}$ iii) $y = \overline{A \cdot B}$. **(08 Marks)**

8 a. What is the latch-up problem that arises in bulk CMOS technology? **(08 Marks)**

b. Give any 5 guide lines for avoiding latch-up. **(05 Marks)**

c. With aid of diagram explain the performance modeling procedure. **(07 Marks)**

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